

AMENDMENT

Please amend the application as follows:

In the Specification:

Please replace the paragraph at page 1, lines 14-19 with the following paragraph:

This patent application claims priority to Provisional U.S. Patent Application Serial No. 60/261,506, Attorney Docket No. SILA:072PZ1, filed on January 12, 2001. This patent application further claims priority to Provisional U.S. Patent Application Serial No. 60/273,119, Attorney Docket No. SILA:072PZ2, titled "Partitioned RF Apparatus with Digital Interface and Associated Methods," filed on March 2, 2001. This patent application incorporates by reference the above provisional patent applications in their entirety.

Please replace the paragraph at page 1, lines 21-23 with the following paragraph:

Furthermore, this patent application relates to concurrently filed, commonly owned U.S. Patent Application Serial No. 09/821,342, Attorney Docket No. SILA:072, titled "Partitioned Radio-Frequency Apparatus and Associated Methods," now U.S. Patent No. 6,804,497.

Please amend the paragraph at page 6, lines 7-8 to read as follows:

FIG. 1 illustrates the block diagram of an RF transceiver. The RF transceiver includes radio circuitry that ~~operations~~ operates in conjunction with baseband processor circuitry.

Please amend the paragraph at page 6, lines 16-18 to read as follows:

FIG. 2C illustrates yet another embodiment of RF transceiver circuitry partitioned according to the invention. In this embodiment, the reference generator circuitry resides within the baseband processor circuitry.

Please amend the paragraph at page 12, lines 8-19 to read as follows:

The embodiment 200A in FIG. 2A comprises a first circuit partition, or circuit block, 214 that includes the receiver analog circuitry 208 and the transmitter circuitry 216. The embodiment

200A also includes a second circuit partition, or circuit block, that includes the receiver digital ~~receiver~~ circuitry 212. The embodiment 200A further includes a third circuit partition, or circuit block, that comprises the local oscillator circuitry 222. The first circuit partition 214, the second circuit partition 212, and the third circuit partition 222 are partitioned from one another so that interference effects among the circuit partitions tend to be reduced. The first, second, and third circuit partitions preferably each reside within an integrated circuit device. In other words, preferably the receiver analog circuitry 208 and the transmitter circuitry 216 reside within an integrated circuit device, the receiver digital circuitry 212 resides within another integrated circuit device, and the local oscillator circuitry 222 resides within a third integrated circuit device.

Please amend the paragraph at page 14, line 16 to page 15, line 7 to read as follows:

FIG. 3 shows the mechanisms that may lead to interference among the various blocks or components in a typical RF transceiver, for example, the transceiver shown in FIG. 2A. Note that the paths with arrows in FIG. 3 represent interference mechanisms among the blocks within the transceiver, rather than desired signal paths. One interference mechanism results from the reference signal 220 (*see* FIGS. 2A-2D), which preferably comprises a clock signal. In the preferred embodiments, the reference generator circuitry produces a clock signal that may have a frequency of 13 MHz (GSM clock frequency) or 26 MHz. If the reference generator produces a 26 MHz clock signal, RF transceivers according to the invention preferably divide that signal by two to produce a 13 MHz master system clock. The clock signal typically includes voltage pulses that have many Fourier series harmonics. The Fourier series harmonics extend to many multiples of the clock signal frequency. Those harmonics may interfere with the receiver analog circuitry 208 (*e.g.*, the low-noise amplifier, or LNA), the local oscillator circuitry 222 (*e.g.*, the synthesizer circuitry), and the transmitter circuitry 216 (*e.g.*, the transmitter's voltage-controlled oscillator, or VCO). FIG. 3 shows these sources of interference as interference mechanisms 360, 350, and 340.

Please amend the paragraph at page 36, line 19 to page 37, line 11 to read as follows:

The receiver digital circuitry 905 communicates with the receiver analog circuitry 910 via configurable interface signal lines 945. Interface signal lines 945 preferably include four configurable signal lines 950, 955, 960, and 965, although one may use other numbers of configurable signal lines, as desired, depending on a particular application. In addition to supplying

the serial interface signals 920, the baseband processor circuitry 120 provides a control signal 915, shown as a power-down (PDNB) signal in FIG. 9A, to both the receiver digital circuitry 905 and the receiver analog circuitry 910. The receiver digital circuitry 905 and the receiver analog circuitry 910 preferably use the power-down (PDNB) signal as the control signal 915 to configure the functionality of the interface signal lines 945. In other words, the functionality of the interface signal lines 945 depends on the state of the control signal 915. Also, the initialization of the circuitry within the receive path and the transmit path of the transceiver occurs upon the rising edge of the PDNB signal. Note that the PDNB signal is preferably an active-low logic signal, although one may use a normal (*i.e.*, an active-high) logic signal, as persons skilled in the art would understand. Note also that, rather than using the PDNB signal, one may use other signals to control the configuration of the interface signal lines 945, as desired.

Please amend the paragraph at page 37, lines 13-21 to read as follows:

In the power-down or serial interface mode (*i.e.*, the control signal 915 (for example, PDNB) is in the logic low state), interface signal line 950 provides the serial clock (SCLK) and interface signal line 955 supplies the serial interface enable signal (SENB). Furthermore, interface signal line 960 provides the serial data-in signal (SDI), whereas interface signal line 965 supplies the serial data-out signal (SDO). During this mode of operation, the transceiver may also perform circuit calibration and adjustment procedures, as desired. For example, the values of various transceiver components may vary over time or among transceivers produced in different manufacturing batches. The transceiver may calibrate and adjust its circuitry to take those variations into account and provide higher performance.

Please amend the paragraph at page 40, line 13 to page 41, line 6 to read as follows:

FIG. 9B shows an embodiment 900B that includes a configurable interface according to the invention. Here, the baseband processor circuitry 120 subsumes the functionality of the receiver digital circuitry 905. The baseband processor circuitry 120 realizes the functionality of the receiver digital circuitry 905, using hardware, software, or both, as desired. Because the baseband processor circuitry 120 has subsumed the receiver digital circuitry 905, the baseband processor circuitry 120 may communicate with the receiver analog circuitry 910 using configurable interface signal lines 945, depending on the state of the control signal 915 (*e.g.*, the PDNB signal). The configurable

interface signal lines 945 perform the same functions described above in connection with FIG. 9A, depending on the state of the control signal 915. As noted above, one may reconfigure the interface signal lines 960 and 965 during transmit mode to implement desired functionality, for example, logic signals.

Please amend the paragraph at page 42, line 13 to page 43, line 8 to read as follows:

Interface controller circuitry 1010 provides as output signals a receiver digital circuitry SDO signal 1018, a select signal 1020, and an enable signal 1022. The receiver digital circuitry SDO signal 1018 represents the serial data-out signal for the receiver ~~analog~~ digital circuitry 905, *i.e.*, the serial data-out signal that the receiver digital circuitry 905 seeks to provide to the baseband processor circuitry 120. The interface controller circuitry 1010 supplies the select signal 1020 to multiplexer circuitry 1014. The multiplexer circuitry 1014 uses that signal to selectively provide as the multiplexer circuitry output signal 1024 either the receiver digital circuitry SDO signal 1018 or the receiver analog circuitry SDO signal 1044, which it receives through configurable interface signal line 965. Tri-state driver circuitry 1016 provides the multiplexer circuitry output signal 1024 to the baseband processor circuitry 120 under the control of the enable signal 1022.

Please amend the paragraph at page 48, line 16 to page 49, line 6 to read as follows:

FIG. 11B illustrates a block diagram of a preferred embodiment 1100B of a delay-cell circuitry 1119 according to the invention. The delay-cell circuitry 1119 includes a replica of the clock driver circuitry 1114A in tandem with a replica of the data receiver circuitry 1120A. (Note that the delay-cell circuitry 1119 may alternatively include a replica of the data driver circuitry 1154 in tandem with a replica of the clock receiver circuitry 1130.) The replica of the clock driver circuitry 1114A accepts the clock signal 1112A and the complement clock signal 1112B. The replica of the clock driver circuitry 1114A provides its outputs to the replica of the data receiver circuitry 1120A. The replica of the data receiver circuitry 1120A supplies the clock signal 1121A and the complement clock signal 1121B. The clock signal 1121A and the complement clock signal 1121B constitute the output signals of the delay-cell circuitry 1119. The delay-cell circuitry 1119 also receives as inputs enable signals 1118 and 1124 (note that FIG. 11A does not show those input signals for the sake of clarity). The enable signal 1118 couples to the replica of the clock driver

circuitry 1114A, whereas the enable signal 1124 couples to the replica of the data receiver circuitry ~~1124A~~ 1120A.

Please amend the paragraph at page 49, line 19 to page 50, line 2 to read as follows:

The receiver digital circuitry 905 and the receiver analog circuitry 910 preferably reside within separate integrated-circuit devices. Because those integrated-circuit devices typically result from separate semiconductor fabrication processes and manufacturing lines, their process parameters may not match closely. As a result, the preferred embodiment 1100B of the delay-cell circuitry 1119 does not compensate for the delay in the clock receiver circuitry 1130, the data driver circuitry 1154, and the data receiver circuitry 1120 in FIG. 11A.

Please amend the paragraph at page 50, lines 4-16 to read as follows:

Note, however, that if desired, the delay-cell circuitry 1119 may also compensate for the signal delays of the clock receiver circuitry 1130, the data driver circuitry 1154, and the data receiver circuitry 1120. Thus, in situations where one may match the process parameters of the receiver digital circuitry 905 and the receiver analog circuitry 910 relatively closely (for example, by using thick-film modules, silicon-on-insulator, etc.), the delay-cell circuitry 1119 may also compensate for the delays of other circuit blocks. As another alternative, one may use a delay-cell circuitry 1119 that provides an adjustable delay and then program the delay based on the delays in the receiver digital circuitry 905 and the receiver analog circuitry 910 (*e.g.*, provide a matched set of receiver digital circuitry 905 and receiver analog circuitry 910), as persons skilled in the art would understand. Furthermore, rather than an open-loop arrangement, one may use a closed-loop feedback circuit implementation (*e.g.*, by using a phase-locked loop circuitry) to control and compensate for the delay between the receiver analog circuitry 910 and the receiver digital circuitry 905, as desired.

Please amend the paragraph at page 50, lines 18-21 to read as follows:

Note that the digital circuit blocks shown in FIGS. 11A and 11B depict mainly the conceptual functions and signal flow. The actual circuit implementation may or may not contain separately identifiable hardware for the various functional blocks. For example, one may combine the functionality of various circuit blocks into one circuit ~~blocks~~ block, as desired.

Please amend the paragraph at page 53, lines 12-17 to read as follows:

FIG. 13 shows a schematic diagram of a preferred embodiment 1300 of a signal-receiver circuitry according to the invention. One may use the signal-receiver circuitry as the clock receiver circuitry 1130 and the data receiver circuitry 1120 in FIG. 11A. In the latter case, the input signals to the signal-receiver circuitry constitute the ~~IOP~~ ION and ~~ION~~ IOP signals 960 and 965 and the enable signal 1124, whereas the output signals constitute the signals at the outputs 1122A and 1122B, respectively, in FIG. 11A.

Please amend the paragraph at page 58, lines 13-18 to read as follows:

Furthermore, as noted above, one may use the partitioning and interface concepts according to the invention not only in RF transceivers, but also in RF receivers for high-performance applications. In such RF receivers, one may partition the receiver as shown in FIGS. 2A-2D and 4-8, and as described above. In other words, the RF receiver may have a first circuit partition that includes the receiver analog circuitry, and a second circuit partition that includes the receiver digital circuitry.